FIXED PULSE-WIDTH 10-TAP MILLISECOND TIMER (SERIES 3D3250)

RoHS Compliant

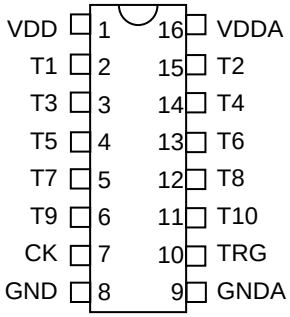
data delay devices, inc.

FEATURES

- All-silicon, low-power CMOS technology
- CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- **Timer range:** 160ns through 16.0ms
- **Output Pulse Width:** Equal to one clock period
- **Temperature/Vdd stability:** Equal to that of reference clock
- **Minimum input pulse width:** 10.0ns

For mechanical dimensions, click here.
For package marking details, click here.

PINOUT



3D3250-xx DIP-16
3D3250R-xx SOIC-16

FUNCTIONAL DESCRIPTION

The 3D3250 10-tap timer is designed for use in applications that require long yet very precise time intervals. Upon receipt of a trigger, the device generates 10 pulse outputs, spaced equally in time. The output-to-output time spacing is equal to the product of the input clock period and the device dash number. The stability of the timer is thus limited only by the stability of the reference clock. Each output consists of a pulse whose width is equal to one period of the reference clock. The 3D3250 is offered in a standard 16-pin auto-insertable DIP and a space saving surface mount 16-pin SOIC package.

PIN DESCRIPTIONS

TRG	Trigger Input
CK	Clock Input
T1-T10	Timer Outputs
VDD	+3.3 Volts
VDDA	+3.3 Volts
GND	Ground
GNDA	Ground

TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	OUTPUT-TO-OUTPUT SPACING (us)				
	REF CLK = 31.25 MHz	REF CLK = 40.00 MHz	REF CLK = 50.00 MHz	REF CLK = 62.50 MHz	REF CLK = 80.00 MHz
3D3250-5	0.160				
3D3250-10	0.320	0.250	0.200		
3D3250-20	0.640	0.500	0.400	0.320	0.2500
3D3250-25	0.800	0.625	0.500	0.400	0.3125
3D3250-50	1.600	1.250	1.000	0.800	0.6250
3D3250-100	3.200	2.500	2.000	1.600	1.2500
3D3250-200	6.400	5.000	4.000	3.200	2.5000
3D3250-250	8.000	6.250	5.000	4.000	3.1250
3D3250-500	16.00	12.50	10.00	8.000	6.2500
3D3250-1K	32.00	25.00	20.00	16.00	12.500
3D3250-2K	64.00	50.00	40.00	32.00	25.000
3D3250-2.5K	80.00	62.50	50.00	40.00	31.250
3D3250-5K	160.0	125.0	100.0	80.00	62.500
3D3250-10K	320.0	250.0	200.0	160.0	125.00
3D3250-20K	640.0	500.0	400.0	320.0	250.00
3D3250-25K	800.0	625.0	500.0	400.0	312.50
3D3250-50K	1600.0	1250.0	1000.0	800.0	625.00

NOTE: Any dash number between 5 and 50K not shown is also available as standard.

APPLICATION NOTES

OPERATIONAL DESCRIPTION

The 3D3250 timer waveforms are shown in Figure 1. The device is composed of a number of timers connected in series. Each timer produces at its output a signal with a fixed pulse width (equal to one period of the reference clock), shifted in time. The timers are matched and share the same compensation signals, which minimize output-to-output deviations over temperature and supply voltage variations.

INPUT TRIGGER CHARACTERISTICS

The period of the input signal (TRG) must be, at a minimum, 200ns greater than the total time of the particular device. This determines the highest input frequency for guaranteed reliable device operation. The input pulse width must also be greater or equal to 10ns.

INPUT CLOCK CHARACTERISTICS

The input reference clock frequency determines the device timing specifications and provides a very stable reference to the compensation circuitry to mitigate power supply and temperature timing variations. The 3D3250 operates with an input reference clock that can range from 31.25 MHz to 80 MHz. The clock may run asynchronously with respect to the trigger input. Table 1 tabulates total delays only at preselected clock frequencies.

The device total time and the output-to-output (incremental) times are multiples of the input clock period as per the following equations:

$$T_I = T_{CK} * \text{DashNumber}$$

$$T_{TOTAL} = T_I * 10$$

For example, a 3D3250D-250, when operated with a 40MHz (25ns period) reference clock, will have an increment of 6.25us (25ns x 250) and a total time of 62.5us.

CONSIDERATIONS

The device timing accuracy and stability stem from the frequency source driving the 3D3250 delay line. Therefore, the input clock signal must have excellent frequency accuracy through power supply and temperature excursion. More importantly, a frequency source with the minimum possible short and long term jitter specifications should be selected.

The device has two power (VDD & VDDA) and two ground (GND & GNDA) pins. The VDD and GND pins power the digital circuitry while the VDDA and GNDA pins power the analog circuitry within the device. Bypass of the power pins is highly recommended, especially the VDDA pin. High frequency lay-out techniques are encouraged to be employed.

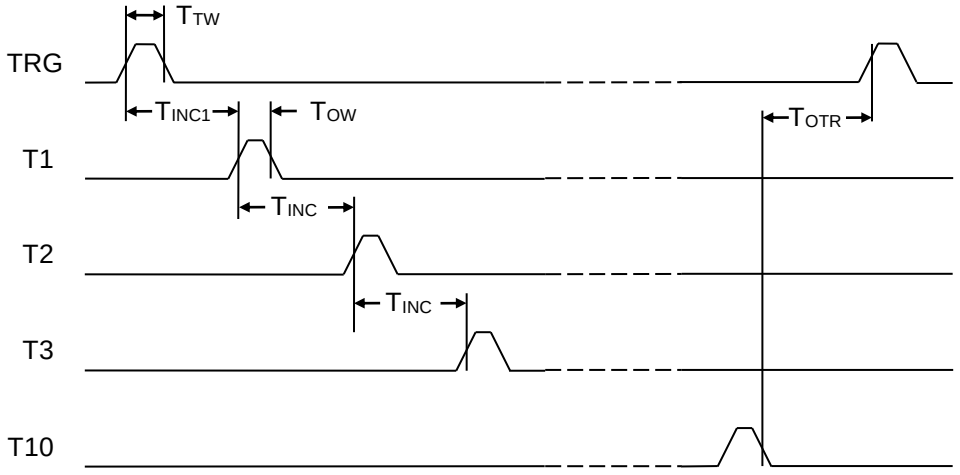


Figure 1: Timing Diagram

DEVICE SPECIFICATIONS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-1.0	1.0	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		20	35	mA	
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}			1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}			1.0	µA	$V_{IL} = 0V$
High Level Output Current	I_{OH}		-15.0	-4.0	mA	$V_{DD} = 3.0V$ $V_{OH} = 2.4V$
Low Level Output Current	I_{OL}	4.0	15.0		mA	$V_{DD} = 3.0V$ $V_{OL} = 0.4V$
Output Rise & Fall Time	T_R & T_F		2.0	2.5	ns	$C_{LD} = 5$ pf

TABLE 4: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Input Reference Clock	f_{CK}	31.25		80	MHz	1
Reference Clock Duty Cycle	DC(f_{CK})	40		60	%	
Trigger Pulse Width	T_{TW}	10			ns	
Output-to-Output Time Delay	T_{INC}		T_I		ns	2
Input-to-Output1 Time Delay	T_{INC1}	T_I + 50		T_I + 65	ns	3
Output-to-Output RMS Delay Jitter			80		ps	4
Input-to-Output RMS Delay Jitter (any tap)			650		ps	4
Output Pulse Width	T_{OW}		1		T_{CK}	
Output to Trigger Recovery Time	T_{OTR}	200			ns	
Output Rise & Fall Time	T_R & T_F		2.0	2.5	ns	

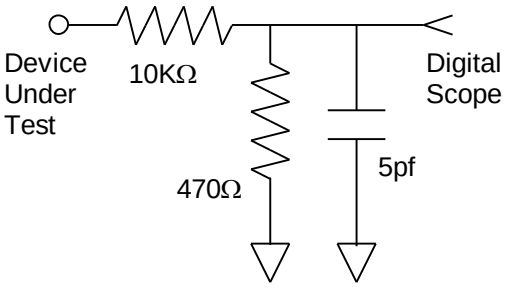
1. The clock frequency is restricted for smaller dash numbers (see Table 1)
2. $T_I = T_{CK}$ * DashNumber, where $T_{CK} = 1 / f_{CK}$
3. The difference between T_{INC1} and T_{INC} depends on T_{CK}. Roughly, T_{INC1}-T_{INC} = 68ns - T_{CK}/2
4. This is the jitter introduced by the device and does not include any jitter introduced by the reference clock

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25ºC ± 3ºC
Supply Voltage (Vcc): 3.3V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: PW_{IN} = 20 ns
Period: PER_{IN} = 1.5 x Total Delay

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

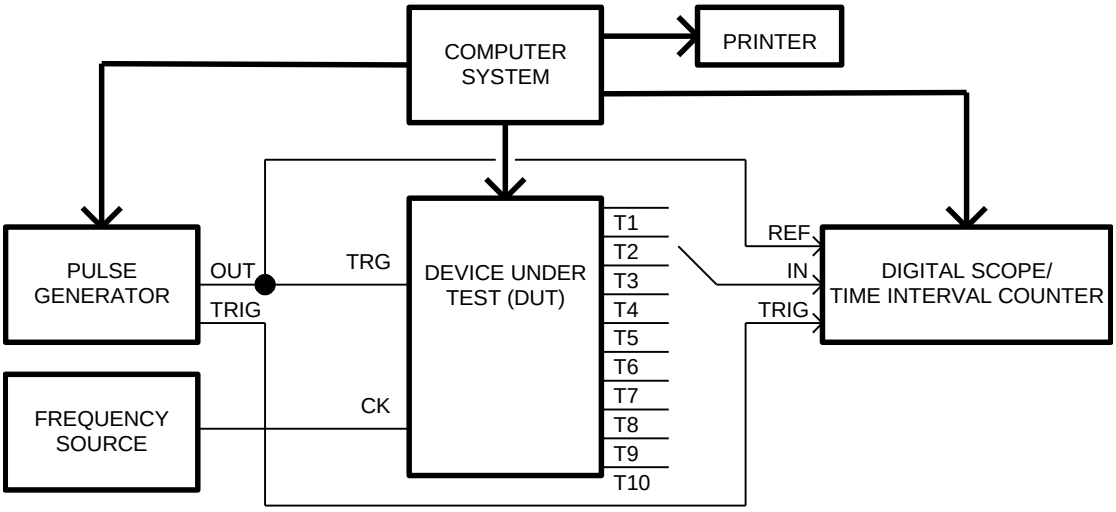


Figure 2: Test Setup

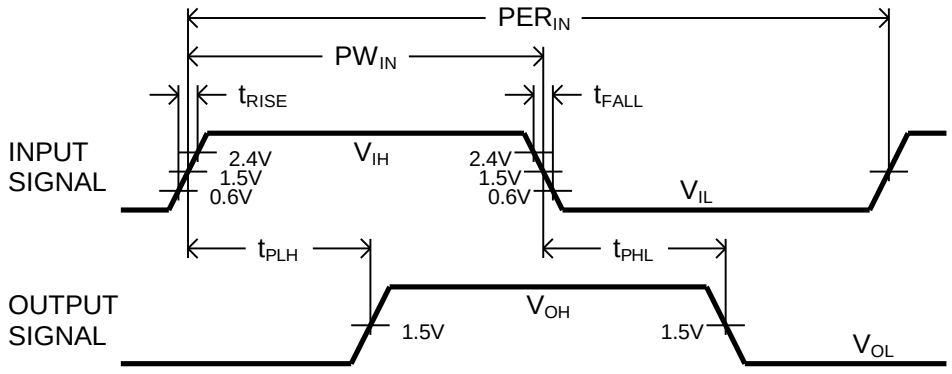


Figure 3: Timing Diagram